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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,957	07/30/2003	Kevin J. Ryan	303.519US2	8890

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,957	RYAN, KEVIN J.	
	Examiner	Art Unit	
	Kee M Tung	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-24* is/are rejected.

7)☒ Claim(s) *3 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment and response filed 11/19/04 have been considered in preparing this Office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 5, 7-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al (5,754,838) in view of IBM (16 Mb Double Data Rate Synchronous Graphics RAM hereinafter "IBM").

Shibata et al teaches a SDRAM device (Fig. 2) comprising a controller (212) for controlling the operation mode of the SDRAM includes a mode register (30; col. 5, lines 53-62) and a control logic (col. 4, lines 47-59); a data input buffer (210); a memory array (200A and 200B); capable of operating over wide range of operation frequencies with a change-over circuit for changing the range of variable frequencies of the PLL circuit or changes the variable frequencies of the DLL circuits based upon mode setting information fed from mode register (abstract). Shibata et al further teaches "in alternately, the operation of the PLL circuit or the DLL circuit may be halted (disables PLL or DLL) in the testing mode permitting the clock signals fed through the external terminal to pass through so as to use them as internal clock signals. Such a testing

mode can be conveniently set by the mode register." (col. 15, lines 3-7). However, Shibata fails to explicitly suggest or teach a DDR SDRAM/SGRAM and use different modes for the DLL/PLL circuit. IBM teaches a **bi-directional data strobe double data rate (DDR) SGRAM** (pages 1 and 4) comprising a memory array including a quad-bank DRAM (page 4, shows 4 512 x 256 x 32 memory banks) having full page burst capability (page 1, col. 1); a mode register (pages 4 and 6) for storing operating modes of SGRAM (includes two DLL modes, a normal or activate modes, and non-DLL modes, such as, TM mode, BT mode, CAS latency mode and Burst length mode) and a DLL circuit (page 4). The DLL can be set and reset for normal and activate operations and further can be internally disable (such as, during self refresh operation on page 21) and enable (other operations) during certain operations. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of IBM into the system of Shibata et al in order to provide a high speed bi-directional data strobe DDR SGRAM (or SDRAM with graphics features) because the DDR SGRAM of IBM is an improvement of the SDRAM of Shibata for high speed access (at least from single data rate to double data rate). Therefore, at least claims 1-24 would have been obvious.

Allowable Subject Matter

4. Claims 3 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 11/19/04 have been fully considered but they are not persuasive.

It seems to the examiner that applicant argues limitations that are not in the claims. The Specification is not the measure of invention. Therefore, limitations contained therein cannot be read into the claims for the purpose of avoiding the prior art. In re Sporck, 55 CCPA 743, 386 F .2d 924, 155 USPQ 687 (1968). In this case, the claims merely require a DLL or PLL capability in a first mode and a non-DLL or non-PLL capability in a second mode. Both prior art clearly teaches or suggest a second mode other than the DLL or PLL capability mode. In prior art to Shibate, even if the non-PLL or non-DLL mode is in a test mode, as long as the mode is not a DLL or PLL mode. The claims should be interpolated in broadly by any other mode. Similarly, in prior art to IBM, applicant argues that the non-DLL mode is only to the memory refresh mode when internally disabling the DLL (which can be interpolated as in a non-DLL mode).

Regarding arguments to provide "alignment of output data on a read line of the memory", it was old and well know in the art that the DLL or PLL capability provides for the feature. Since both Shibate and IBM teach or suggest at least the DLL or PLL capability mode, the feature would have been obvious. Similarly this also applies to non-DLL or non-PLL capability mode. Since they don't have the DLL or PLL capability, they are not aligned. I guest this is also the reason why applicant didn't give any teachings or supports in the specification for how to provide the alignment of an output data on a read line in DLL or PLL capability mode. How DLL/PLL and Non-DLL/non-PLL capability modes are related to a different alignment? The only area of the specification mention about this feature is last paragraph on page 6 and the paragraph

bridge between pages 6 and 7 in one sentence and read as "DLL or PLL capability generally provides for alignment of an output data on a read line." Therefore, for at least the reasons set forth above, applicant's arguments are not deemed to be persuasive.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2676